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## Frequency, delay and velocity analysis for intrinsic channel region of carbon nanotube field effect transistors

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Gate wrap around field effect transistor is preferred for its good channel control. To study the high frequency behaviour of the device, parameters like cut-off frequency, transit or delay time, velocity are calculated and plotted. Double-walled and array of channels are considered in this work for enhanced output and impedance matching of the device with the measuring equipment terminal respectively. The performance of double-walled carbon nanotube is compared with single-walled carbon nanotube and found that the device with double-wall shows appreciable improvement in its characteristics. Analysis of these parameters are done with various values of source/drain length, gate length, tube diameters and channel densities. The maximum cut-off frequency is found to be 72.3 THz with corresponding velocity as  $5 \times 10^6$  m/s for channel density as 3 and gate length as 11nm. The number of channel is varied from 3 to 21 and found that the performance of the device containing double-walled carbon nano tube is better for channel number lesser than or equal to 12. The proposed modelling can be used for designing devices to handle high speed applications of future generation.

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### 1. Introduction

Besides being smaller in size, carbon nanotube field effect transistor (CNTFET) gives high performance in its device applications. CNT has its distinctive electronic and mechanical properties allowing us to provide high speed and low power consumption devices. The compact sized transistor fits for high level integration. CNTs are formed by rolling graphene sheets to a tube shape and their conducting character (semiconductor or metal) depends upon the direction of rolling called chirality. Semiconducting carbon nanotube is used to design high frequency transistors keeping the tube as the channel.

Somani et.al experimented whether single-walled CNTFET would undergo type conversion (from p- to n-) when subjected to vacuum annealing. They absorbed and found that single wall carbon nano tube with high work function metals as contacts, will not experience type conversion when it is cycled between air and vacuum. Fabrication of such stable devices is easier and it is obtained by careful selection of tube diameter [1]. CNTFETs shows high ON state and Off state according to Joerg Aenzeller. There are two ways to improve the high frequency performance of CNTFETs, one is by scaling down the device dimensions and other is by increasing the mobility of charge carriers [2].

High frequency performance of CNTFET is explored by Hamieh [3] using a compact model for single-wall channelled CNTFETs. For MOSFET-like CNTFET, the cut off frequency is very low due to larger

parasitic capacitances of the device. The parasitic effect can be greatly reduced with an array of parallel channels instead of single channel between the source and drain electrode supporting the increase in cut off frequency. The work involves quasi-state approach for studying the high frequency performance of the device and cut off frequency ( $f_T$ ) is found to be 10 GHz. The significance of semiconducting CNTFET is stressed by Henri Happy that it suits for high frequency performance and the device is faster, compared to its conventional counterpart FETs. Impedance mismatch between the carbon Nano tube and radio-frequency equipment is the problem in direct measurement of high frequency for single channel. It is found that it can be overcome by using array of parallel conducting channels that supports for improving impedance matching [4].

David L. Pulfrey reviews [5] the high frequency performance of CNTFET. In his work, Schrodinger and Poisson equations are solved self consistently and the equation for  $f_T$  is extrapolated. It is found that the  $f_T$  depends upon the parasitic capacitances, gate length and source /drain resistance. Also the work states that the values of  $f_T$  can be improved by applying multiple parallel CNT conductors while the band-structure-determined velocity plays an important role in high frequency analysis of CNTFETs. The unity current gain frequency  $f_T$  is predicted by L.C. Castro et.al [6] using small-signal equivalent circuit. Schrodinger and Poisson equations are solved self consistently and showed that the cut off frequency is subjected to change with variation in the gate-bias voltage. Using gate length 2 nm and gate bias dependence,  $f_{Tmax}$  is about 600 GHz which is very low to 4 THz if its bias dependence are ignored.

Cut off frequency is a figure-of-merit in analysing high frequency performance characteristics of transistors. Expressions for maximum operating frequency which suits a wide range of physical properties, parasitic resistances, and gate biases are derived using small signal- equivalent circuit and found that an optimized device design will give  $f_{max} > 0.5$  THz by L.C. Castro et.al [7]. It is found that the limitation of cut off frequency is the domination of larger parasitic capacitance value over gate-to-gate capacitance or gate-source capacitance in single channel carbon nanotube FETs. D. Wanget.al in their work calculated  $f_T$  as 0.2 GHz with parasitic capacitance and it is 10GHz without the parasitic effect [8]. So, the performance after de-embedding the parasitic capacitance is excellent but, it has to be included in real circuit.

Carrier transit delay analysis of graphene field effect transistor is the work done by Han Wanget.et.al [9]. Cut off frequency for  $L_g=210$  nm is found to be 18 GHz and 22 GHz before and after de-embedding the parasitic capacitance respectively. The separation of total delay into intrinsic, extrinsic and parasitic optimizes the RF device structure. David L. Pulfrey et.al [10] analysed the signal delay at high frequency for a gate wrap around CNTFET containing single wall tube. Effective mass Schrodinger and Poisson equations are solved self- consistently for a tube of (11,0) chirality. It is found that the overall delay is due to device tunnelling in the channel region and modulation of the space charge in source and drain regions. It is predicted that for lowest sub band,  $V_{gs}=(0.4-0.7)$  V,  $V_s = 0.7$  V, the cut off frequency is  $f_1= 47$  THz,  $\tau=3.4$  fs and the velocity  $v = 2 \times 10^6$  m/s.

Multi-wall CNTs possesses low resistance, shorter delay and easy to fabricate. The gate is wrapped around the tube for it gives good channel control [11 - 12].

In this research work, frequency, delay and velocity of gate wrap around double walled array CNTFET are analysed. The cut off frequency ( $f_T$ ), the signal delay ( $\tau$ ) and the propagation velocity in the intrinsic channel region ( $v$ ) are calculated for different gate, source/drain length values. The response of the above key operating parameters are plotted and studied for different tube diameters and channel densities.

**2. Analysis:**

The effect of parasitic capacitances - both fringe and gate-substrate capacitance on gate channel capacitance are included for an array of parallel channels connected between source and drain regions. The chiralities of inner and outer walls are taken as (26,0) and (17,0) respectively. The channel length is taken as 16 nm and source/drain length as 32 nm. The dependence of cut off frequency on various parameters like gate, source/drain length are discussed. Figure 1. illustrates the double-wall channelled gate wrap around CNTFET. The source and drain regions of the device are heavily doped and the channel region is intrinsic.

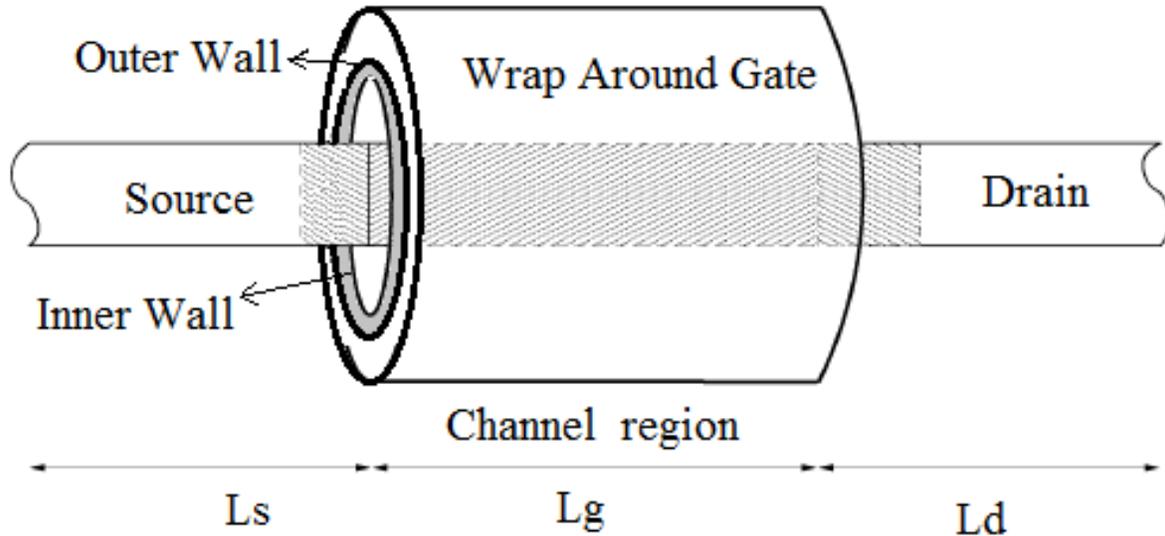


Figure.(1) : Illustration of double wall channelled gate wrap around CNTFET.

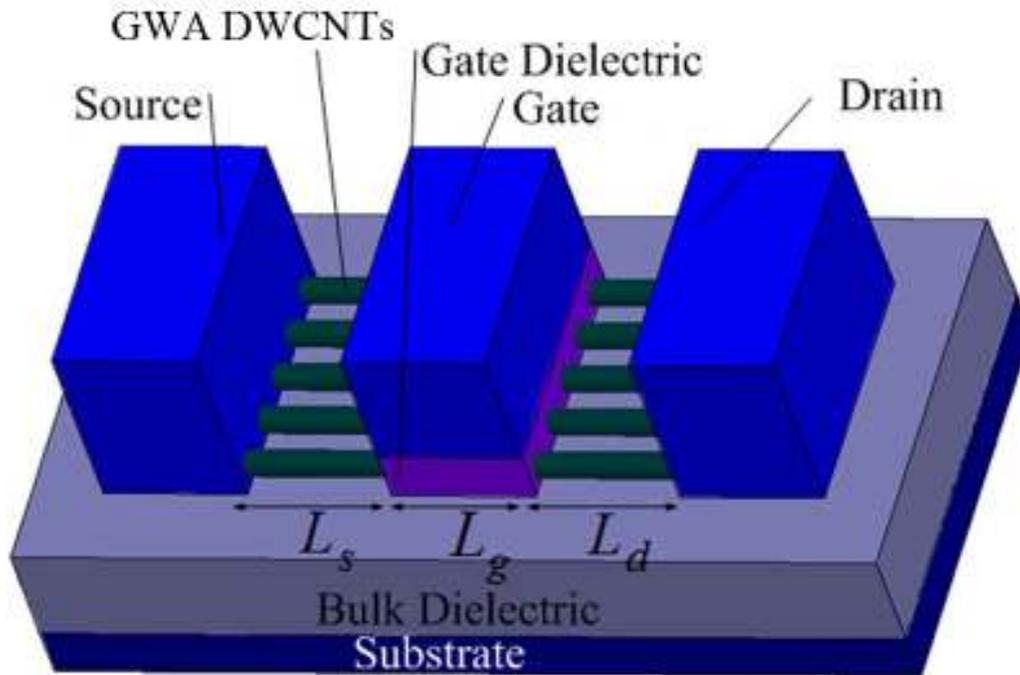


Figure (2) : Illustration of Gate wrap around array DWCNTs.

Figure (2) illustrates the 3-D view of the device with array of double walled channels wrapped around by the gate similar to the structure presented in [11]. Array of parallel conductors produce screening and imaging effects both due to neighbouring channels and inter wall interference. All such effects are taken into account while calculating the capacitances. Also, the effect of the adjacent channels on the end channels at one side and the middle channels at both the sides are included. Number of channels assumed in this work is three, while the number of walls are two(outer and inner) with corresponding outer and inner tube diameter as 2.0 nm and 1.34 nm. The gate, fringe, substrate, and coupling capacitances are derived and calculated using equations from [11] and [12]. The value of these capacitances are used to find the drive capacitance (C), and charge of the individual tubes ( $Q_{wall}^{(o/i)}$ ) both outer and inner. Equations from (1) to (4) are solved simultaneously for surface potential of outer and inner walls.

$$Q_{cap,o/i} = C_{gc,o/i}(V_G - V_{FB}) + C_{sub,o/i}V_{sub} + C_{c,o/i}\beta_{o/i}V_{ch,D,o/i} + C_{c,o/i}(1 - \beta_i)V_{ch,S,o/i} - (C_{gc,o/i} + C_{sub,o/i} + C_{c,o/i})\frac{\Delta\phi_{B,o/i}}{e} \tag{1}$$

$$Q_{wall,s/d}^{(o/i)} = 4\frac{e}{L_x} \sum_{m=1}^M k_m^{(o/i)} \sum_{l=0}^L k_l^{(o/i)} \left[ \frac{1}{\frac{(E_{m,0}^{(o/i)} - \Delta\phi_B^{(o/i)})}{1+e} - \frac{\Delta\phi_B^{(o/i)}}{kT}} \right] \tag{2}$$

$$Q_{wall}^{(o/i)} = Q_{wall,s}^{(o/i)} + Q_{wall,d}^{(o/i)} \tag{3}$$

$$Q_{cap,o/i} = Q_{wall}^{(o/i)} \tag{4}$$

where,  $k$  - Boltzmann constant  
 $T$  - Kelvin temperature.

$C_{c,o}(C_{c,i})$  - Coupling capacitance of the outer (inner) wall due to surface potential.

$Q_{cap,o/i}$  - Charge induced on the electrodes per unit length and

$Q_{wall}^{(o/i)}$  - Charge induced on both the outer and inner walls.

The drive current and drive capacitance [11] are found from the following equations,

$$I = \min(N, 2) \cdot (I_s^{(o)} + I_s^i) + \max(N - 2, 0) \cdot (I_m^{(o)} + I_m^i) \tag{5}$$

$$C = C_g L_g + f_{millier} \cdot 2 \left( C_{of}^{(g)} L_s + C_{gs} W_{pitch} \right) + C_{gsub} \tag{6}$$

The relation for cut off frequency  $f_T$  is taken from [5, 6, 11]

$$f_T = \frac{g_m}{2\pi C} \quad (7)$$

where, 
$$g_m = \frac{\partial I}{\partial V_G} \quad (8)$$

$I$ - drive current

$C$  -drive capacitance.

The total signal delay time ' $\tau$ ' is inversely proportional to the cut off frequency  $f_T$ . The signal delay  $\tau$  is found from the following equations [9 - 11].

$$\tau_{total} = \frac{1}{2\pi f_T} \quad (9)$$

The signal propagation velocity in the intrinsic channel region  $v_{Fermi}$  is calculated from [5]

$$v_{Fermi} = L_g \times 2\pi f_T \quad (10)$$

### 3. Results and Discussions:

The objective behind the results specified here, is to project the aptitude of the proposed model in finding the useful and important estimates of the key parameters for studying the high frequency performance of carbon nanotube with wrap around gate transistors. Device containing double-walled CNT is the simplest of all Multi-wall channelled CNTs and the merits of the same is shown with the following outcomes. The Cut-off frequency ( $f_T$ ) is the figure-of-merit which is very significant while studying the device high frequency performance characteristics. Here, the response of high frequency is plotted for various key parameters like tube diameters ( $d$ ), channel densities ( $N$ ), source/drain length ( $L_{sd}$ ) and last but very importantly the gate length ( $L_g$ ). The signal propagation time ( $\tau$ ) is the transit time from one end to the other of the channel. It is checked for the same set of above parameters. The velocity of propagation ( $v_{Fermi}$ ) is the speed of the transit time crossing the intrinsic channel region. It is the product of cut-off frequency ( $f_T$ ) and the gate length ( $L_g$ ). Cut-off frequency, delay and velocity are plotted for diameters  $d=1.6\text{nm}$ ,  $2.0\text{ nm}$ ,  $2.4\text{ nm}$ ,  $2.8\text{ nm}$  (chiralities= [(35,0),(19,0)], [(26,0),(17,0)], [(31,0), (16,0)], [(35,0), (22,0)]). Cut-off frequency and delay time ratio are plotted against gate length ( $L_g$ ) for comparing the performance of the devices with double and single-walled channel for the chirality (26,0), (17,0).

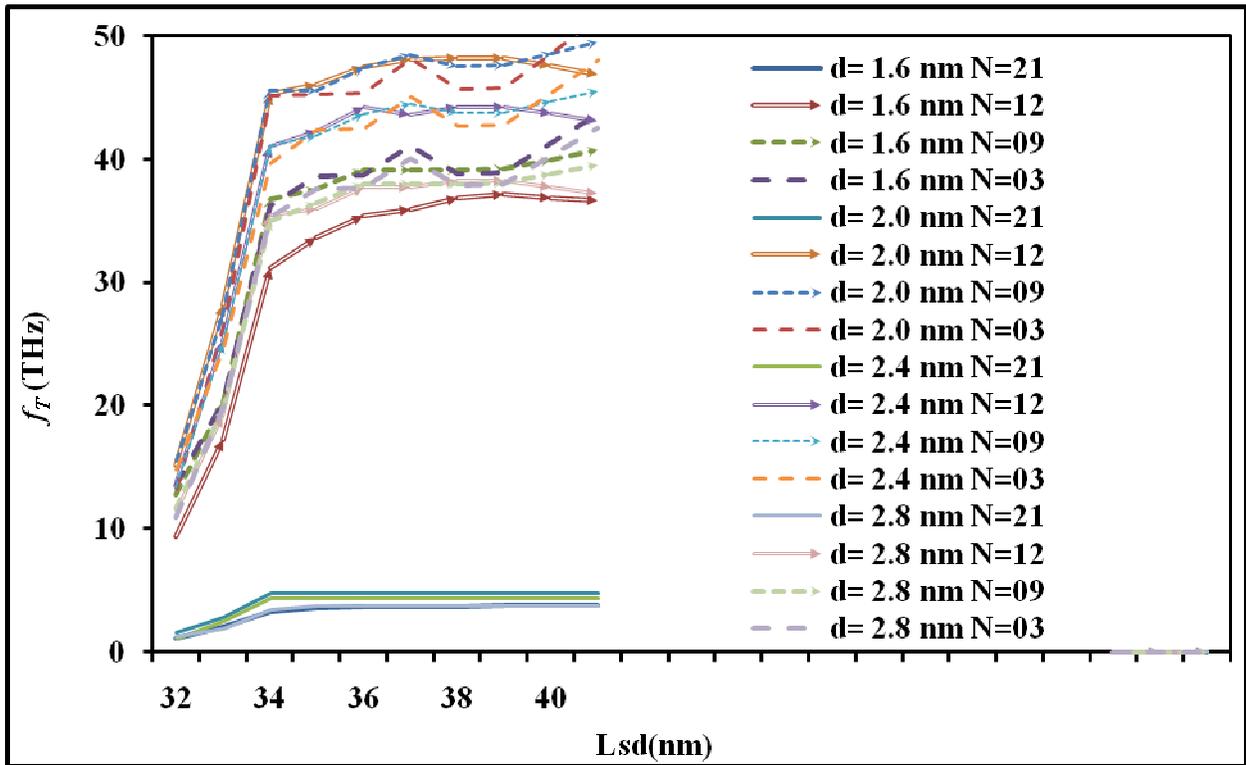


Figure (3) : High frequency response for change in source/drain length with various diameters and channel densities.

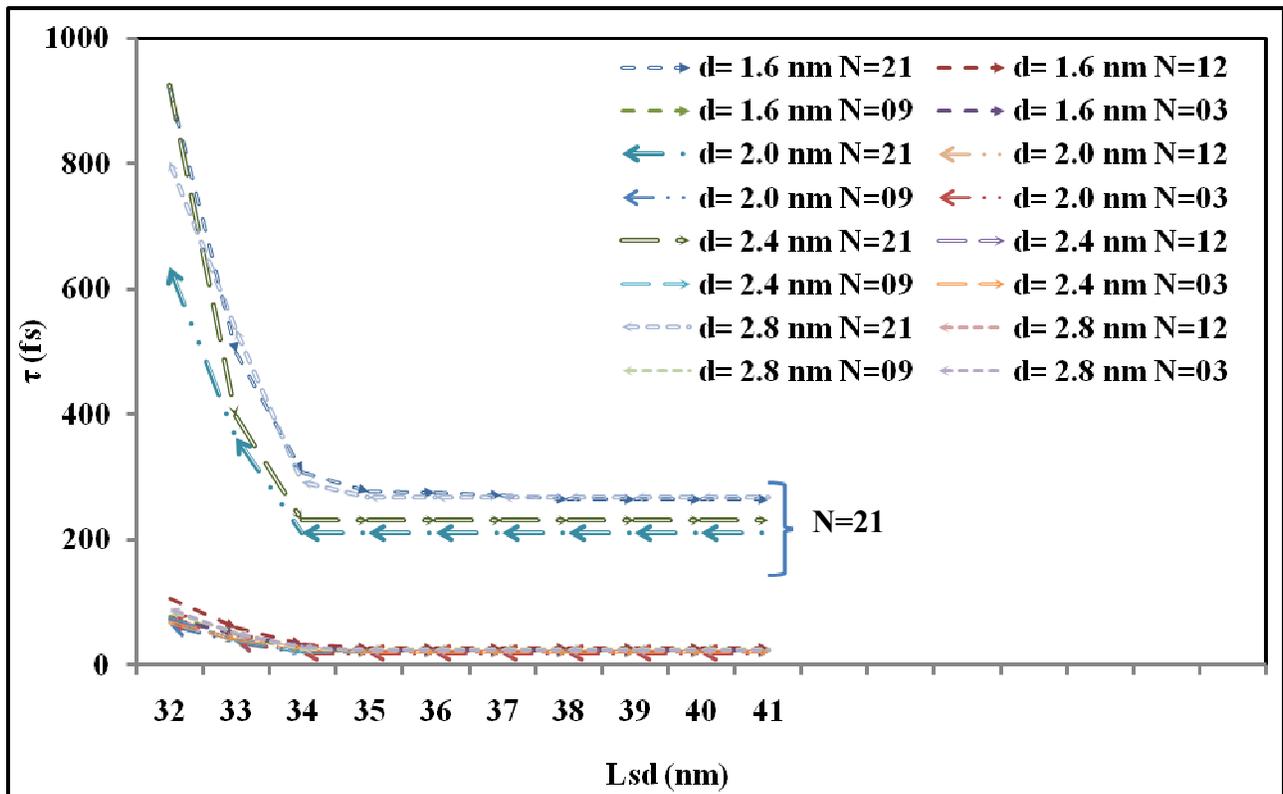


Figure (4) : Delay response with respect to source and drain length variation for various value of diameters and channel densities.

The cut-off frequency is calculated by taking the ratio of change in drive current with respect to the gate-bias. It is required to study the frequency response of the device with respect to source/drain length. Also, it is equally significant to know the response of the same parameter for different diameters of the Carbon nano tube and different number of channels wrapped by the gate. Figure (3) depicts the plot of the figure-of-merit for the change of above parameters. From the graph, it is understood that the curve increases linearly till the value of Lsd is 34 nm after which it remains constant. The linearity is more for  $N \leq 21$  with constant value. The cut-off frequency ranges between 35 THz and 48 THz for  $Lsd \geq 34$  nm and for  $N$  lies between 3 & 12 while for  $N=21$ , it is 4.7 THz only. The effect of change in diameter may not be apparent but cannot be negligible for such 1-D devices.

The source/drain length plays an important role to be studied for delay response. Delay time is the reciprocal of cut-off frequency and it is obvious from the Figure (4). For Channel density 21, the delay is greater than other samples of channel densities. It is seen that the delay decreases from 924 fs to 230 fs for  $N \leq 12$  in average for all the diameters taken. It is the lowest for  $N=21$  i.e., equal to 2.0 nm. For diameter 1.6 nm, 2.8 nm the variation coincides because of the chirality taken. (chiralities =  $[(35,0),(19,0)]$ ,  $[(35,0),(22,0)]$ ). It is from 56 fs to 20 fs for the rest of the channel densities and all the diameters considered. After  $Lsd = 34$  nm, the decrement in time delay is almost constant which has to be taken care while designing such small devices.

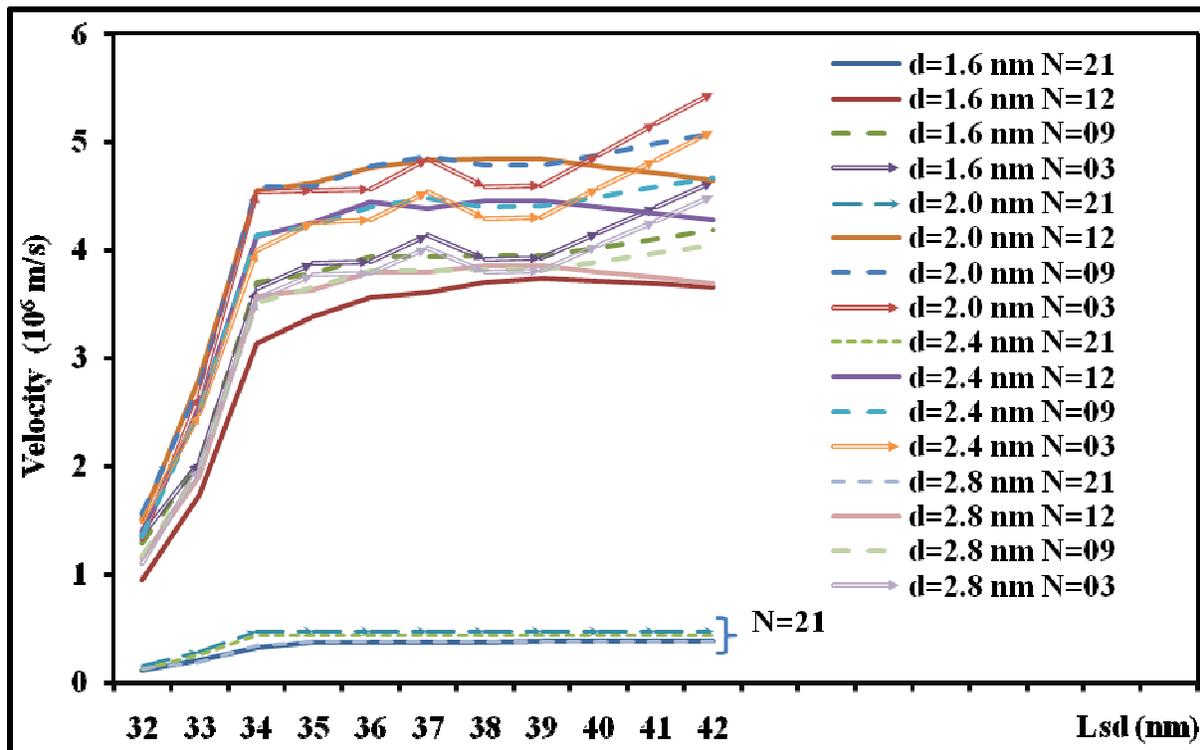


Figure (5) : The variation of velocity with respect to source/drain length for various diameters and number of channels.

Cut-off frequency is directly related to the intrinsic channel region velocity of the device. The Fermi velocity is plotted against source/drain length in Figure (5). It is checked for various channel densities and diameters of the channel. It is found that velocity is lower for  $N=21$ , more or less the same velocity for other samples of 'N' taken. The Fermi velocity starts from  $1.7 \times 10^6$  m/s for  $d=1.6$  nm,  $Lsd = 32$  nm,  $N=12$  and after reaching  $Lsd = 34$  nm, more or less a constant velocity persists for all N's and d's other than  $N=21$ . The velocity is  $0.4 \times 10^6$  m/s for  $N=21$ , all diameters for  $Lsd \geq 34$  nm. It is concluded that number of channels can be limited to 12 so as to get good velocity performance of the device.

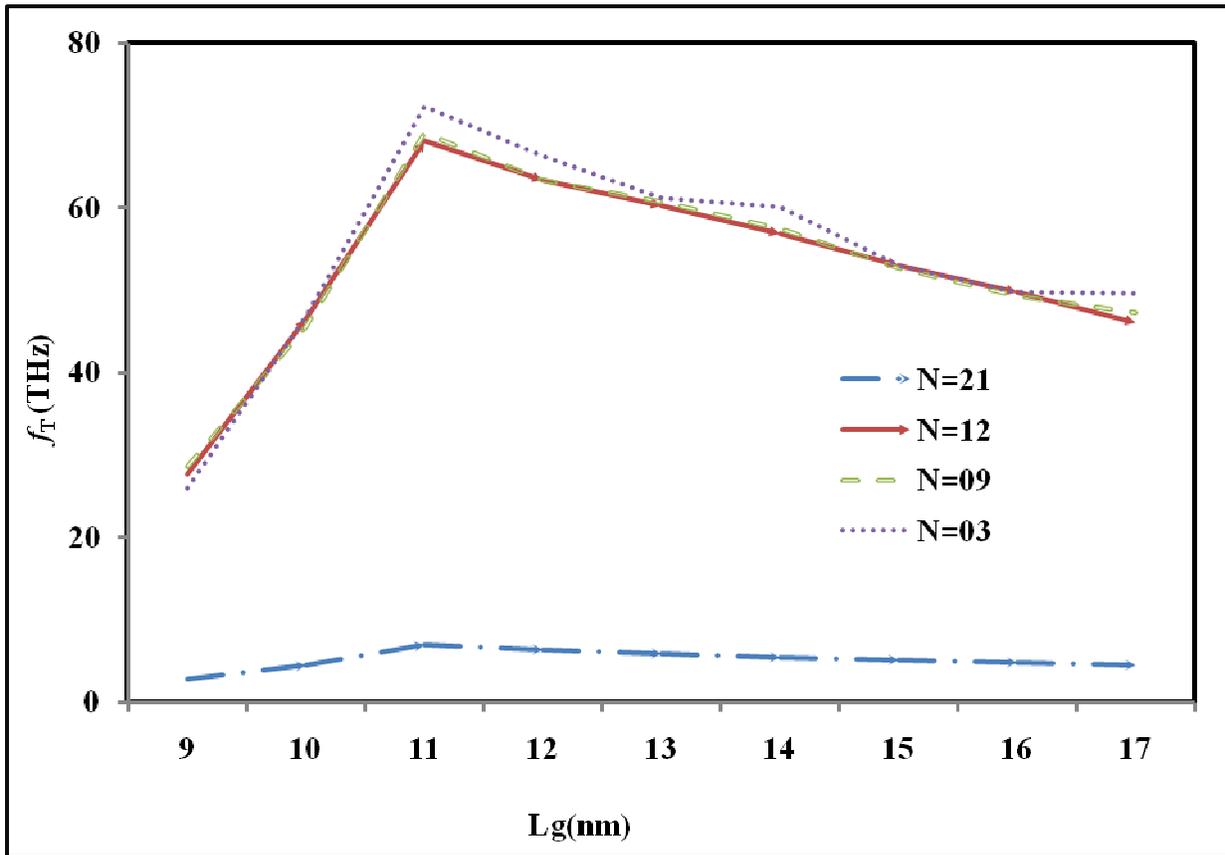


Figure (6) : Response of cut-off frequency with respect to gate length and number of channels.

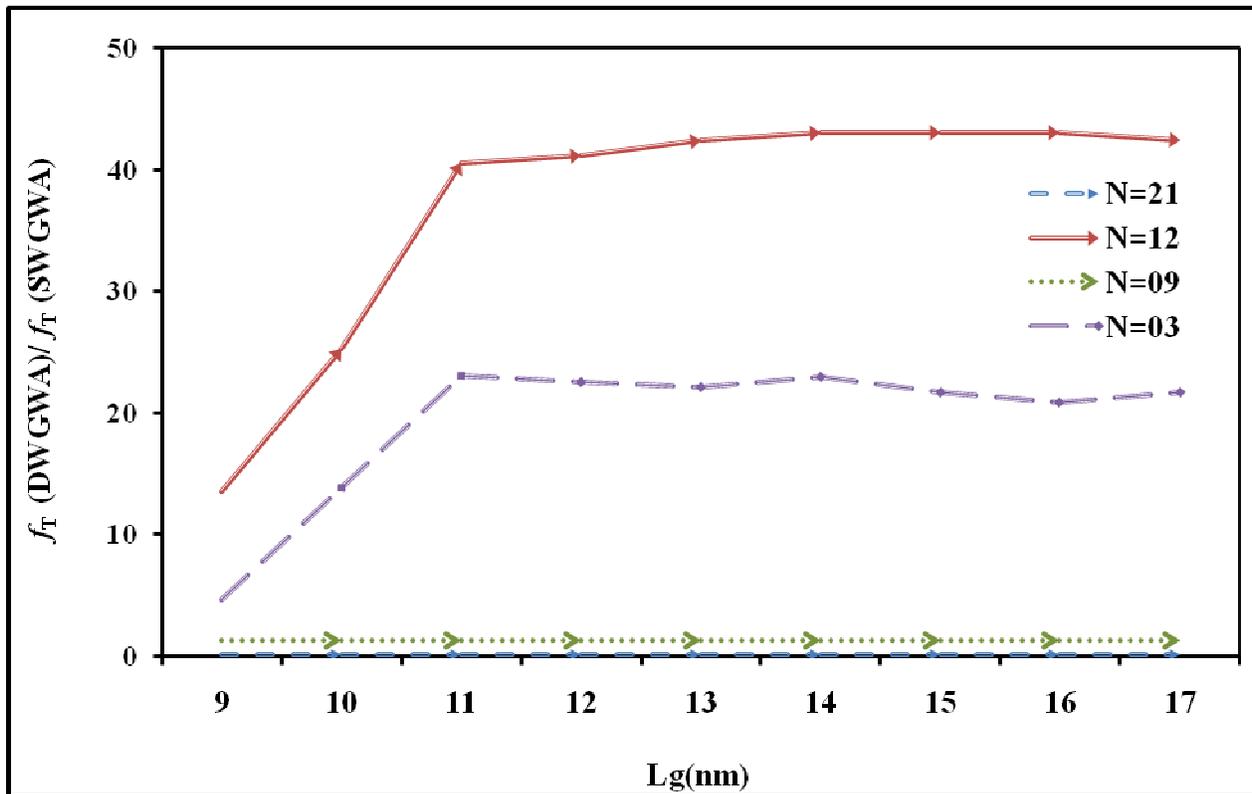


Figure (7) : Cut-off frequency ratio for double-wall and single-wall channelled device with respect to various gate length and number of channels.

The cut-off frequency is drawn for  $d=2.0\text{nm}$ , various values of gate length and for  $N=3, 9, 12$  &  $21$ . From the Figure (6), it is apparent that the cut-off frequency increases and reaches maximum at  $L_g=11\text{ nm}$  and the increment slope is greater than decrement slope after the maximum cut-off frequency. If the values are compared for number of channels, the maximum response is  $7\text{ THz}$  for  $N = 21$  and around  $70\text{ THz}$  for  $N=3, 9$  &  $12$  at  $L_g=11\text{ nm}$ . As the gate length increases, cut-off frequency decreases with increase in channel density. The cut-off frequency calculated here includes all the parasitic capacitances. If calculated de-embedding the parasitic effects,  $f_T$  will be still more. But, it is essential not to de-embed them since, they cannot be separated for array of channels as well as multi-wall channels.

The performance improvement study of high frequency response with respect to gate length for device containing double-walled over single-walled channel is important to know the betterment of the proposed device. Comparison of cut-off frequency for both the cases is shown in the Figure (7). For  $N=3$  &  $12$ , the graph shows a linear increment till  $L_g=11\text{ nm}$  and remains almost constant for the rest of the gate length values. It also shows  $1.5$  improvement for  $N=9$  and no improvement for  $N=21$ . Increasing the channel density above  $12$  is not supporting the cut-off frequency improvement for double-walled channelled device since it provides more screening effects. The screening effects and or imaging effects includes both due to neighbouring channels and due to individual walls of the channels. So, the number of channels can be limited to twelve.

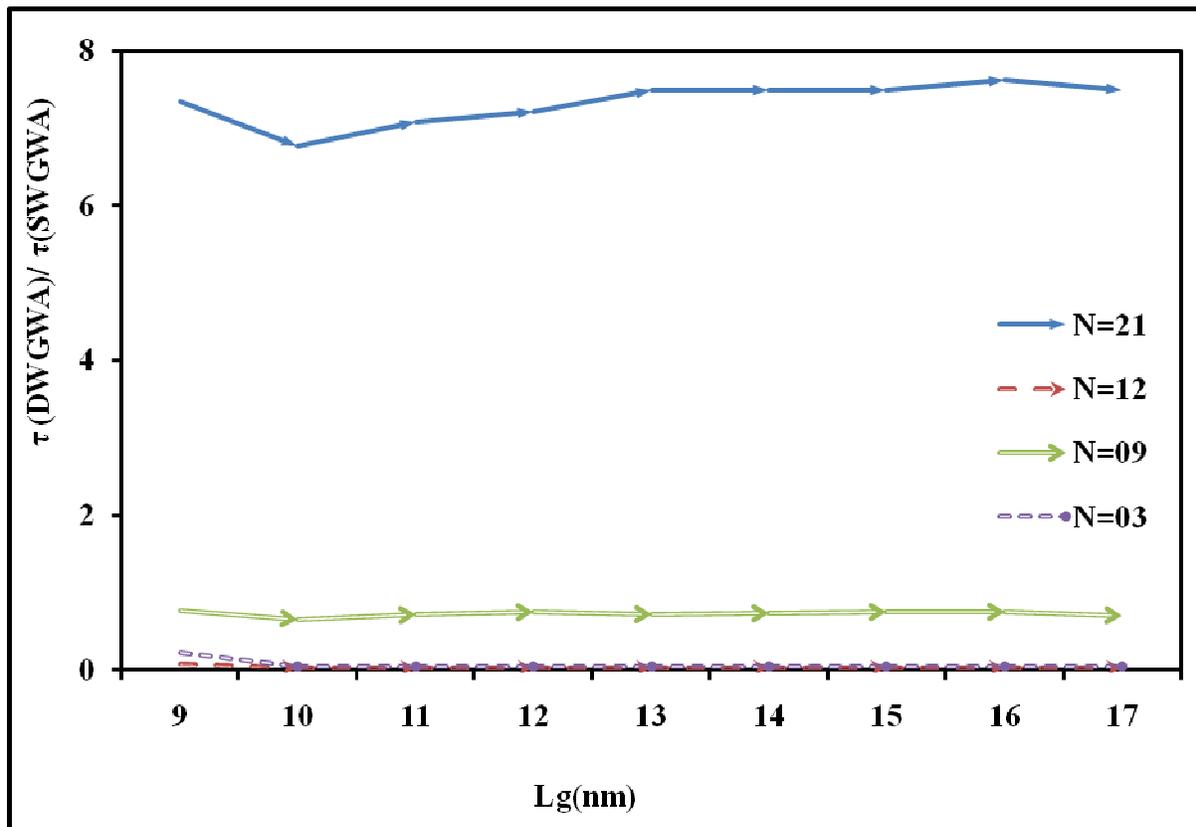


Figure (8) : Delay time variation with respect to gate length for various channel density.

Though the transport through the channel is ballistic instead of diffusive, the study of delay time provides information regarding the transit speed of the charge carriers. The graph shows the performance improvement of delay time response of double-walled device over single-walled transistor in Figure (8). The variation of delay time with respect to channel length is plotted for  $N=3, 9, 12$  and  $21$ . From the graph it is found that, more the number of channels, more the delay time. For  $N=3, 12$  the improvement is negligible, for  $N=9$  it is  $0.7$ , for  $N=21$  it is around  $7.5$ . Delay ratio shows no

improvement for  $N \leq 12$  for the device containing double-wall over its counterpart. Mobility of the charge carriers is limited due to scattering mechanisms like impurity, optical and phonon scattering. Delay can be improved by increasing the gate bias voltage and by using different substrate material to manage the scattering effects.

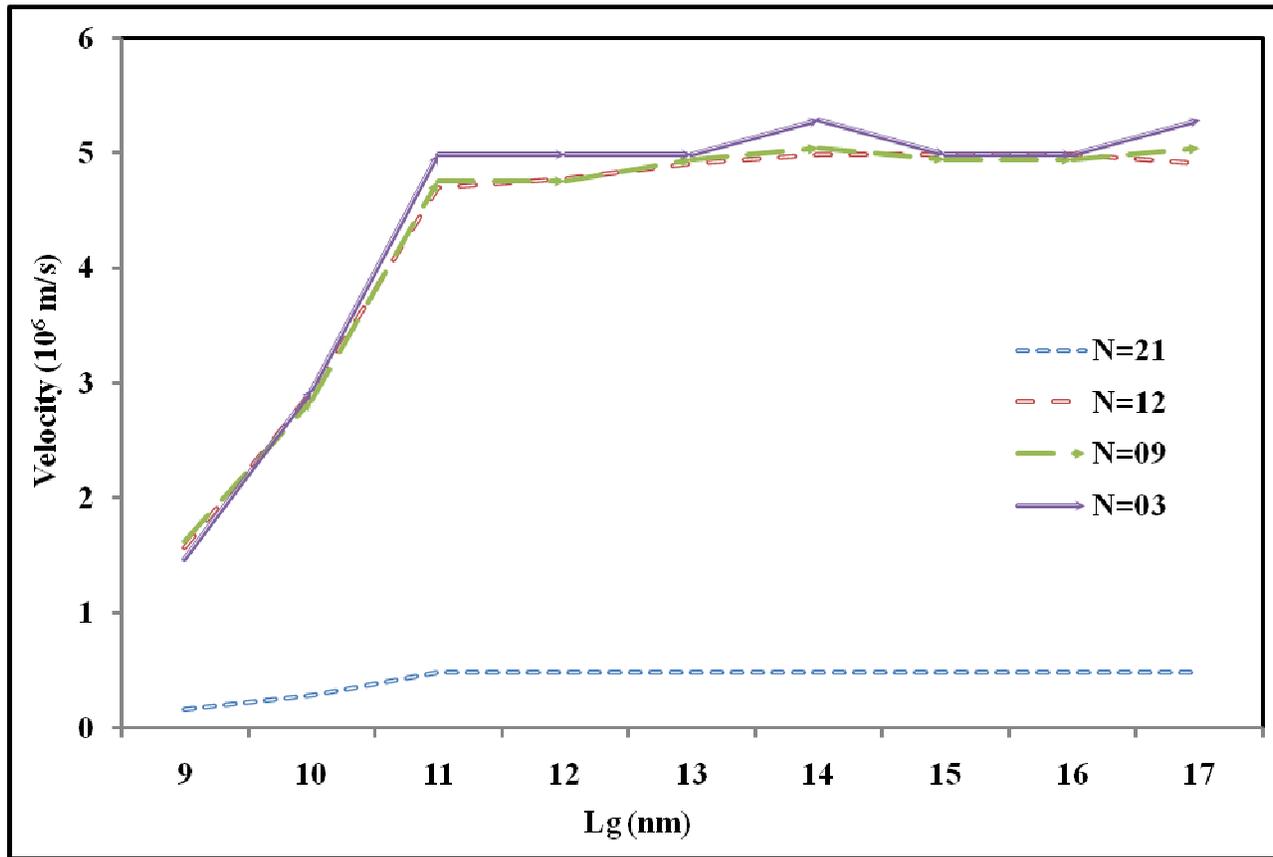


Figure (9) : The response of gate length with respect to velocity for various channel densities.

The channel velocity of the charge carriers is plotted against the gate length variation in the Figure (9). The graph shows minimal change for  $N=21$ , more the channel density, lesser the velocity. The response of velocity for  $N=21$  is lower, it is around  $0.4 \times 10^6$  m/s for gate length greater than 11 nm while it is  $4.7 \times 10^6$  m/s for same gate length, diameter and for  $N \leq 12$ . The velocity curve increases linearly from  $1.4 \times 10^6$  m/s to  $4.7 \times 10^6$  m/s for  $L_g=9$  nm through 11 nm and remains almost constant for  $L_g \geq 11$  nm. But for  $N=21$ , the increment is very little,  $v=0.48 \times 10^6$  m/s for  $L_g=11$  nm. The reason behind the constant velocity is ballistic transport. The cause of brake down at  $L_g=11$  nm is that the cut-off frequency is maximum at this point.

## Conclusions

The response of Cut –off frequency, delay time and velocity are calculated for various channel densities, diameters of channels wrapped in the gate, source/drain length and gate length. High 'k' dielectric ( $\text{HfO}_2$ ) is placed for oxide media between the channels and the wrapping gate. Single channel suffers from impedance mismatching with measuring equipment terminal. To enhance the impedance matching of the carbon nanotube with the terminal of the measuring equipment, an array of parallel tubes are considered to be wrapped inside the gate of the proposed double-wall channelled transistor. More the number of channels, more will be the screening and or imaging effects due to nearby channels as well as the individual channel walls. All the factors are to be taken while planning for high frequency

devices. The result shows remarkable performance for  $N \leq 12$ , 72.3 THz is the maximum cut-off frequency found for  $N=3$ ,  $L_g= 11$  nm, while the velocity is  $5 \times 10^6$  m/s. Though Delay ratio with respect to gate length is not favouring double-walled device over that of single-walled for  $N \leq 12$ , it is better for higher values of  $N$ . There should be a trade-off consideration while designing such devices. It is concluded that Double-Walled Gate Wrap around Array Carbon Nano Field Effect Transistor performs better with higher cut-off frequency, higher velocity and shorter delay time which can be utilized for designing high speed device applications.

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